



PG1 - Multicore implementation

This course tackles multicore implementation issues

Objectives

- This course describes the multiple types of multicore implementations : SMP, AMP.
- It details the hardware resources required to support SMP.
- Debug issues are also studied.
- ACSYS offers a large set of multicore processor trainings: ARM Cortex-A9MP (reference R6), Freescale MPC8641D (reference FC5) and MPC8572E (reference FN10).

A more detailed course description is available on request at info@ac6-formation.com

Prerequisites

- Knowledge of high-end processor cores is recommended.

Plan

MULTIPROCESSING TYPES

- AMP
- SMP
- BMP
- Applications examples (MPC8641D, MPC8572, Virtex-4, Virtex 5)

HARDWARE REQUIREMENTS

- Exclusive resource management
- MMU page descriptor table, PowerPC tbsync instruction
- Multi-core interrupt controller
- Inter-Processor Interrupts
- Message passing

MULTITASK IN MULTI-CORE SYSTEMS

- System booting
- Defining shared resources and non-shared resources
- Assigning a number to each core
- Dispatching tasks to a particular core, static approach, dynamic approach
- I/O management, consequence on driver design

CACHE COHERENCY

- Software coherency (Power instructions dcbz, dcbf, dcbi, icbi)
- Hardware coherency : snooping
- Distinguishing two types of cache enabled area : random access vs sequential access, NUMA model

IMPLEMENTING A MULTI-CORE SYSTEM IN A XILINX VIRTEX-4 FX / VIRTEX-5 FXT FPGA

- PLB basics
- Exclusive resource management, lwarx/stwcx.
- Implementing a multi-core interrupt controller
- Synchronizing time bases
- Is SMP possible in a multi-405 FPGA ?

Renseignements pratiques

Duration : 2 days
Cost : 1250 € HT



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Last site update: Tue 22 May 2012 10:50:29 CEST

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