



MV1 - MARVELL MV6446X implementation

This course covers Marvell Discovery III devices

Objectives

- The course describes the MV6446X internal data paths.
- The course explains how the host PowerPC and a CPU connected to PCI-X can synchronize to each other through the message unit.
- A long introduction to DDR SDRAM is done prior to describe the DDR SDRAM controller operation.
- The course focuses on the hardware implementation of the DDR SDRAM.
- The training explains how to implement chained DMA transfers, by using either IDMA channels or XOR engines.
- The course highlights the possible optimizations that can be implemented to boost the performance of the Ethernet controller.
- This course has been delivered several times to companies developing defence and avionics systems.

A more detailed course description is available on request at info@ac6-formation.com

Prerequisites

- Knowledge of PowerPC 60X / MPX bus. See our courses on Freescale and IBM Microelectronics PowerPCs.

Related courses

- Ethernet and switching, reference [N1](#)
- PCI, reference [IC1](#)
- PCI-X, reference [IC3](#)

Plan

OVERVIEW

- 5-bus architecture, organization of a board based on MV6446X
- Frequency domains, fast path between CPU and SRAM / SDRAM
- Data integrity checking
- Internal crossbar
- Headers retarget

CPU INTERFACE

- CPU address space decoding
- CPU-to-PCI address remapping
- Arbitration, multi-processor operation

- Cache coherency
- Transaction ordering
- Hardware implementation

INTEGRATED SRAM

- Functional description, SRAM access arbitration
- Write-Through vs CopyBack coherency
- ECC protection

DDR INTERFACE

- Introduction to DDR SDRAM from Jedec specification
- Initialization sequence
- Page management
- Read and write transactions
- Transaction ordering
- Cache coherency
- ECC and read-modify-write transactions
- Hardware implementation, SSTL technology

DEVICE CONTROLLER

- Functional description, transaction queue, read and write data buffers
- Connecting 8/16/32 bit devices
- Timing parameters
- External acknowledgement
- Pack / unpack and burst support

PCI INTERFACE

- PCI bus arbitration
- Master operation in PCI and PCI-X mode
- Target operation in PCI and PCI-X mode
- PCI-to-PCI configuration transactions
- Address decoding
- Cache coherency
- Messaging unit

GENERAL PURPOSE INPUT/ OUTPUT PINS

- Pin direction and polarity definition
- Interrupt request inputs
- Multi Purpose Pin multiplexing

INTERRUPT CONTROLLERS AND TIMERS

- Watchdog timer
- Timers / counters
- Interrupt controller functional description

TWSI CONTROLLER AND RESET

- Master and slave operation, 7- or 10-bit addressing
- Master write sequence, master read sequence
- Slave write sequence, slave read sequence
- Reset pins and configuration

- Serial ROM initialisation
- Requirement for an external Central Resource CPLD

IDMA CHANNELS

- IDMA address decoding
- Demand mode
- Normal mode vs chained mode
- Channel activation

XOR ENGINES

- State machine : Active, Inactive and Paused states
- XOR, CRC and DMA operation modes, format of transfer descriptors
- Memory Initialization operation mode
- ECC error cleanup operation mode
- Address decode windows
- Address override capability
- Cache coherency

MULTI-PROTOCOL SERIAL CONTROLLERS

- Address decoding
- Pinout, connection to MPP logic
- Baud Rate Generator
- MPSC clocking
- SDMA operation
- Transmit descriptor format, ring organization
- Receive descriptor format, ring organization
- HDLC mode, UART mode, Transparent mode

GIGABIT ETHERNET CONTROLLERS

- Interface to the PHY
- Dedicated DMA
- Transmit weighted round-robin arbitration
- Backpressure mode
- Transmit and receive sequences
- Management interface
- MIB
- Synchronous FIFO interface
- DMA operation

Renseignements pratiques

Duration : 4 days
Cost : 1950 € HT



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