



## M1 - 405GP implementation

This course covers AMCC 405GP processor

### Objectives

- The course explains how to design a 405GP based board.
- The SDRAM controller is viewed in detail.
- A boot firmware that initializes the MMU has been developed.
- The course provides an example of interrupt handler that supports nesting.
- External control of DMA channels working in scatter / gather mode is described.
- The course explains the fast ethernet controller operation.
  
- This training has been delivered several times to companies developing embedded systems based on 405GP (Defence systems, multimedia systems).
  
- A chapter on Linux porting can be appended on request.

*Labs are compiled with Diab Data compiler and run under Lauterbach debugger.*

*A more detailed course description is available on request at [info@ac6-formation.com](mailto:info@ac6-formation.com)*

### Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.
- Knowledge of PCI bus is recommended (see our course reference [IC1](#)).

### Plan

#### INTRODUCTION TO 405GP

- Internal bus organization : PLB, OPB, DCR
- Internal concurrent transfers examples
- 405GP CPU board architecture examples
- 405GP mapping

#### THE 405 CORE

- 5-stage pipeline operation
- Speculative execution, guarded memory, SGR register
- Serialization
- Cache basics
- Data flow between external memory and caches
- Memory Management Unit : memory attributes definition (cache enabled / cache inhibited, copyback / writethrough)

- Translation Lookaside Buffer initialization
- Load / store buffer, sync instruction

## **PowerPC ARCHITECTURE FOR EMBEDDED**

- Branch instructions
- Load / store instructions
- Arithmetical and logical instructions, shift and rotate instructions
- The PowerPC EABI
- Cache related instructions
- 16-bit mac instructions to develop fixed point DSP algorithms
- Exception processing
- Critical versus non critical interrupts
- Syndrome registers updating when an exception is taken
- Core timers : PIT, FIT and WDT

## **INTERNAL BUSES**

- PLB bus : transfer protocol, split mode advantage, arbiter initialization
- OPB bus : parking strategy, arbitration
- The PLB-to-OPB bridge
- The DCR bus
- Internal busses related registers initialization
- Bus fault management using syndrome registers

## **CLOCKS, RESET AND POWER MANAGEMENT**

- Clocks synthesizer
- PCI synchronous versus asynchronous mode
- PLL multiplication ratio selection PLLMR and CHCR0 registers initialization
- Low power modes
- The core, chip and system reset effects on 405GP internal resources
- Initialization code example
- 405GP hardware configuration with strap pins

## **INTERRUPT CONTROLLER**

- Interrupt sources enumeration
- Interrupt masking and acknowledgement explanation
- Vectorization mechanism for critical interrupts

## **THE SDRAM CONTROLLER**

- Page mode
- Mode register initialization
- Bank selection and precharge
- SDRAM control truth table
- Chip selection with DQM pins
- Bank activation, read, write and precharge timing diagrams
- ECC error correction
- 405GP SDRAM controller features
- Timing parameters programming

## **THE EXTERNAL BUS CONTROLLER**

- External bus pinout
- Dynamic bus sizing

- Timing parameters initialization in PB0-7AP registers for either bursting or non bursting devices
- Timing diagrams
- External acknowledge with the Ready input
- External master interface : arbitration timing diagram

### THE PCI2.2 BRIDGE

- PCI bridge features
- 405GP as a PCI target
- 405GP as a PCI master
- 405GP as PCI configurator
- Internal arbiter initialization
- 405GP used on a PCI expansion board

### THE 4 DMA CHANNELS

- Burst mode support
- Related signals
- Channels bus priority
- Data packing / unpacking
- Buffers chaining through the scatter / gather mode

### THE FAST ETHERNET CONTROLLER

- Frame description with or without VLAN option
- 405GP Ethernet controller organization
- MII interface
- Hash table disadvantage
- Buffer descriptors management
- Interrupt management

### THE UARTS

- Transmission and reception FIFOs use
- Flow control signals management

### THE IIC INTERFACE

- Protocol basics
- Transfer timing diagrams, IIC SCL and IIC SDA pins
- Transmission and reception sequence

### THE INTERNAL DEBUG TOOLS

- JTAG debug restrictions
- Logic analyser connection through Mictor connectors
- The trace port

## Renseignements pratiques

**Durée : 5 jours**  
**Prix : 2100 € HT**



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