



## **P3 - PPC464 core implementation**

**This course covers the IBM Power 464 core**

### **Objectives**

- A boot firmware that initializes the MMU has been developed to explain the boot sequence.
- Internal debug facilities are described.
- The course focuses on PPC464 low level programming, especially the PowerPC EABI.
- Examples of exception handlers are provided.
- A DFT has been developed to explain how to use MAC instructions.
- The Floating Point Unit operation is described.
- The PLB ports as well as debug related signals are described to facilitate the hardware implementation.
- This course has been delivered several times to engineers developing ASICs based on PPC464.

*Labs are compiled with GNU compiler and run under Lauterbach Trace32 debugger.*

*A more detailed course description is available on request at [info@ac6-formation.com](mailto:info@ac6-formation.com)*

### **Prerequisites**

- Experience of a 32 bit processor or DSP is mandatory.

### **Plan**

#### **INTRODUCTION TO PPC464FP-H90**

- Internal architecture overview
- Highlighting instruction and data paths
- Clocking
- Programming model, the 4 register groups GPRs, SPRs, DCRs and memory mapped
- CoreConnect-based SOCs

#### **THE CORE ARCHITECTURE**

- Pipeline basics
- 7-stage pipeline operation
- Speculative execution, guarded memory
- Serialization
- Cache basics
- Cache programming interface
- Process vs thread

- Memory Management Unit
- 36-bit real address space
- Translation Lookaside Buffer initialisation
- Cache control and debugging features
- Load / store buffer, speculative loads, msync and mbar instructions

### **BOOK E COMPLIANT CORE**

- Booke E objectives
- Branch instructions
- Addressing modes
- Load / store instructions
- Semaphore management with lwarx / stwcx. Instructions
- Arithmetical and logical instructions, shift and rotate instructions
- Floating point unit, compliancy with IEEE754
- Processing denormalized FP numbers
- Floating point arithmetic instructions
- FP-to-integer and integer-to-FP casting
- The PowerPC EABI
- Cache related instructions
- 16-bit mac instructions to develop fixed point DSP algorithms
- 2-cycle multiply option
- Exception processing
- Critical versus non critical interrupts
- Syndrome registers updating when an exception is taken
- Core timers : PIT, FIT and WDT

### **INTEGRATED DEBUG FACILITIES**

- JTAG emulator use
- The 464 instruction trace port
- Real time trace when the PowerPC core executes cached instructions
- Hardware vs software breakpoints

### **HARDWARE IMPLEMENTATION OF THE PPC464 CORE**

- Signal naming convention
- External connections
- Clock and power management interface
- CPU control interface
- Reset interface
- External interrupt controller interface
- Instruction-side PLB interface
- Data-side PLB interface
- DCR interface

## **Renseignements pratiques**

**Duration : 3 days**  
**Cost : 1650 € HT**



SARL au capital de 15400€ - SIRET 449 597 103 00026 - RCS Nanterre - NAF 722C - Centre de Formation : 19, rue Pierre Curie - 92400 Courbevoie  
Siège social et administration : 21, rue Pierre Curie - 92400 Courbevoie - Tél. 01 41 16 80 10 - Fax. 01 41 16 07 78

Last site update: Mon 13 Feb 2012 02:28:18 PM CET

<http://www.ac6-formation.com/>