



## **P2 - PPC440 core implementation**

**This course covers the IBM Power 445 core**

### **Objectives**

- A boot firmware that initializes the MMU has been developed to explain the boot sequence.
- Internal debug facilities are described.
- The course focusses on 440 low level programming, especially the PowerPC EABI.
- Examples of exception handlers are provided.
- A DFT has been developed to explain how to use mac instructions.
- The Floating Point Unit operation is described.
- The PLB ports as well as debug related signals are described to facilitate the hardware implementation.
- This course has been delivered several times to engineers developing ASICs based on PPC440 and to engineers implementing Xilinx FPGAs containing PPC440 core(s).

*Labs are compiled with Diab Data compiler and run under Lauterbach Trace32 debugger.*

*A more detailed course description is available on request at [info@ac6-formation.com](mailto:info@ac6-formation.com)*

### **Prerequisites**

- Experience of a 32 bit processor or DSP is mandatory.

### **Plan**

#### **INTRODUCTION TO 440**

- Internal architecture overview
- Connection to peripheral IPs
- Clocking
- Programming model

#### **THE CORE ARCHITECTURE**

- Pipeline basics
- 5-stage pipeline operation
- Speculative execution, guarded memory
- Cache basics
- Data flow between external memory and caches
- Cache programming interface
- Process vs thread

- Memory Management Unit
- Translation Lookaside Buffer initialisation
- Cache control and debugging features
- Load / store buffer, speculative loads

### BOOK E COMPLIANT CORE

- Book E objectives
- Branch instructions
- Load / store instructions
- Semaphore management with lwarx / stwxc. Instructions
- Arithmetical and logical instructions
- The PowerPC EABI
- Cache related instructions
- 16-bit mac instructions to develop fixed point DSP algorithms
- Exception processing
- Syndrome registers updating when an exception is taken
- Core timers : PIT, FIT and WDT
- Reset

### INTEGRATED DEBUG FACILITIES

- JTAG emulator use
- Real time trace when the PowerPC core executes cached instructions
- Hardware vs software breakpoints

### HARDWARE IMPLEMENTATION OF THE PPC440 CORE

- External connections
- Clock and power management interface
- CPU control interface
- Reset interface
- External interrupt controller interface
- Instruction-side local bus interface
- Data-side local bus interface
- DCR interface

### APU CONTROLLER

- Connection to the native instruction pipeline
- External coprocessor module
- Software interface
- Class of instruction
- Developing a custom instruction set relying on an external coprocessor
- Floating point simple and double precision instructions

## Renseignements pratiques

**Duration : 3 days**  
**Cost : 1650 € HT**



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