



## NS2 - MARVELL 88E6161 Ethernet switches

This course covers Marvell Link Street Gbps Soho switches

### Objectives

- Providing the basic knowledge on 802.3 and 802.1.
- Understanding the parameters that determine the QoS.
- Implementing the Dynamic Queue Limit architecture.
- Description of the Address Lookup engine.
- Implementing the Distributed Switch Architecture.
- Becoming familiar with the API defined by Marvell.
- This course has been delivered several times to companies involved in the design of embedded equipments.

*Practical labs using the Marvell GUI allow attendees to understand the various operation modes offered by this class of switch devices.*

*A more detailed course description is available on request at [info@ac6-formation.com](mailto:info@ac6-formation.com)*

### Prerequisites

- Knowledge of IEEE 802.3 and IEEE 802.1: see our course Ethernet and switching, reference [N1](#)
- Knowledge of IEEE 1588 may also be needed: see our course [N2](#)

### Plan

#### 100 Mbps ETHERNET BASICS

- MAC layer, frame format, frame filtering
- Full duplex Ethernet vs CSMA/CD
- PHY layer, scrambling, 4b/5b coding, NRZI
- Auto-negotiation, utilization of FLPs
- MII

#### 1 Gbps ETHERNET BASICS

- 1000BASE-T
- 1000BASE-X
- GMII transfer protocol, RGMII, SGMII

#### 802.1Q BASICS

- Spanning tree algorithm, RSTP, MSTP
- VLAN tag, selecting one tree and selecting the priority of a frame
- Port states
- Automatic address learning
- Automatic address aging
- Handling multicasts, GVRP, IGMP snooping

### **INTRODUCTION TO 88E6161 SWITCHES**

- Block diagram, ports 0-3 features
- Port 4 and port 5 operating modes
- Pin strapping
- Application examples

### **BASIC SWITCH FUNCTIONS**

- MACs
- PPU
- RMON registers
- Basic switch operation
- 802.1X source address authentication
- Multiple FIDs in VLAN systems

### **NORMAL PORTS**

- Ingress policy
- VLANs
- Special frame handling
- QOS qualification
- Port-based Ingress Rate Limiting
- Queue Controller
- Egress policy

### **PROVIDER PORTS**

- Distinguishing S-TAG from C-TAG
- Customer-to-Provider traffic
- Provider-to-Customer traffic
- Customer-to-Customer traffic
- Provider-to-Provider traffic

### **DSA PORTS**

- Implementing control traffic between switches and management CPU
- Forward DSA tag
- TO\_CPU DSA tag
- FROM\_CPU DSA tag
- Interconnecting switches by using cross-chip links
- Switch handling of DSA frames
- Secure Control Technology

### **ADVANCED SWITCH FUNCTIONS**

- Spanning Tree support
- Ingress MGMT/BPDU frame detection
- Proper connection to a management CPU and to a router
- Port mirroring

- Port trunking support
- PTP implementation

## ACCESSING SWITCH REGISTERS

- The 16 register groups
- Multi-chip addressing mode
- Single-chip direct access to registers
- Remote Management frames

## PHY LAYER

- Transmit PCS and PMA
- Receive PCS and PMA
- Power management
- Far End Fault indication
- Auto MDI/MDIX crossover
- LED interface
- Accessing PHY registers, MDC/MDIO interface
- Auto-configuration

## SOFTWARE ARCHITECTURE

- DSDT suite
- Multi-layer architecture
- OS independency
- Source code organization
- Platform specific routines
- SMI interface functions
- Switch driver layer
- API layer
- Interrupts

## Renseignements pratiques

**Durée : 3 jours**  
**Prix : 1650 € HT**



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