Formation Connectivity - CAN bus: This course covers both CAN bus specification and Freescale / ST CAN bus controllers

IA1 - CAN bus

This course covers both CAN bus specification and Freescale / ST CAN bus controllers

Objectives

- Becoming familiar with CAN 2.0A & 2.0B specifications.
- Parameterizing and using a CAN controller driver for the STM32F2 BxCAN controller
- Testing a CAN system with the assistance of the IXXAT CANAnalyser.

Prerequisites

- Basic knowledge of processor.

Plan

INTRODUCTION

- History
- CAN benefits
- PHY and Link layers features

FRAME ANALYSIS

- Message frames structure
- 2.0A and 2.0B frame description
- Compatibility between both formats

ARBITRATION

- Point to multipoint communication model
- Dominant and recessive states
- Frame priority selection through the label value
- Automatic switch into receive state when an arbitration is lost

TIMING AND SYNCHRONIZATION

- Bit time phases
- Hardware and software resynchronization
- RJW determination

ERROR MANAGEMENT

- The error counter registers
- Error detection areas inside a transmit frame and a receive frame
- Fault confinement
- The 3 states of a CAN node : active, passive and bus off
- Overload frame

CAN NETWORK PERFORMANCE

- The parameters that determine network performance
- Data rate selection
- Distance between both farthest stations
- Connection establishment time

SETTING UP OF A CAN BUS SYSTEM

- Set up of many communications between all CAN stations
- Labs to show the error counter management
- Labs to show the impact of the RJW parameter

CAN SOFTWARE DRIVER DEVELOPMENT

- STM32F2 CAN controller description (BxCAN)
- Label filters configuration through the mask registers
- Bit time phases initialization
- Description of a CAN driver written in C-language

Renseignements pratiques

Durée : 2 jours
Prix : 1250 € HT