



## IC3 - PCI-X 2.0

**This course covers the PCI-X bus version 2.0**

### Objectives

- The course explains the architecture of PCI-X based systems.
- The reset sequence used to select the mode (PCI or PCI-X) and the frequency is detailed.
- The course explains split transactions.
- Transfer protocol is described in details with the assistance of the Lecroy analyser.

*A more detailed course description is available on request at [info@ac6-training.com](mailto:info@ac6-training.com)*

### Prerequisites

- Knowledge of PCI 3.0: see our course reference [IC1](#)

### Plan

#### **INTRODUCTION TO PCI-X**

- PCI restrictions : data rate is not sufficient for Fibre Channel, Ultra SCSI or Gigabit Ethernet applications
- PCI-X technology overview
- Segments and switched fabric
- Relationship between the number of slots and the operation frequency

#### **ELECTRICAL SPECIFICATION**

- Register / register approach, effect on the performance
- Current / voltage curves
- Decoupling rules

#### **PCI-X DEVICE HARDWARE CONFIGURATION AT RESET**

- PCIXCOMP pin utility
- Behavior of a PCI-X motherboard when a PCI board is present
- Behavior of a PCI-X expansion board when it is plugged in a PCI motherboard

#### **TRANSFER PROTOCOL**

- New commands
- Alignment rules

- PCI MEM space address decoding
- Attribute phase
- Split transactions
- Sequence numbering
- Data cachability indication
- Exclusive access
- Arbitration, bus parking

## CONFIGURATION REGISTERS

- Capability list PCI-X structure
- New registers description
- Bus error management

## Renseignements pratiques

**Durée : 2 jours**  
**Prix : 1250 € HT**



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