



## IC1 - PCI 3.0

### This course covers PCI bus version 3.0

#### Objectives

- The training has been designed from the PCI3.0 specification.
- It describes the read prefetch / write posting mechanisms and synchronization rules.
- Transfer protocol is explained with the assistance of the Lecroy analyzer board.
- The course emphasizes the host bridge operation especially the management of PCI accesses targeting cache enabled regions.
- A software routine has been developed to show how to access the configuration space.
- Also interrupt requests allocation, memory regions allocation are detailed in single PCI system and multiple PCI systems (PCI-to-PCI bridge).
- The course explains how to tune the PCI performance: selecting optimized LT value, appropriate master priority, enabling fast-back-to-back.

*A more detailed course description is available on request at [info@ac6-training.com](mailto:info@ac6-training.com)*

#### Prerequisites

- Experience of a digital bus is mandatory
- Experience of a 32-bit processor is recommended

#### Plan

##### OVERVIEW

- PCI specifications history
- PCI bus features
- PCI device types
- Technological introduction
- Architecture of recent PCs

##### PCI DEVICE ARCHITECTURE

- Information buffering
- Buffer management
- Prefetchable vs non-prefetchable memory ranges
- Synchronization rules
- Producer / consumer model
- Optional processings
- PCI bus limitations

## **TRANSFER PROTOCOL**

- Transfer basics
- Pinout, signal classes
- Arbitration
- Data transfer protocol
- Address decoding in IO, MEM and CFG spaces
- 64-bit data transfer
- 64-bit addressing
- Master initiated terminations
- Target initiated terminations
- Fast back-to-back
- Parity control
- Shared resource management
- Bus analyse, benefit of a bus analyser / exerciser

## **INTERRUPTS AND RESET**

- PCI interrupts
- Interrupt acknowledge transaction
- Interrupt sharing
- Message Signaled Interrupts
- MSI-X
- Reset, operating states

## **CACHE COHERENCY**

- Cache basics
- Snooping basics
- Cacheability of RAM accessed by the host CPU through PCI
- PCI masters accessing the host memory
- PCI agent processor accessing the host memory

## **ELECTRICAL SPECIFICATION**

- Switched wave switching vs Incident wave switching
- Static specification
- Dynamic specification : 33 MHz and 66 MHz
- Clocking
- Decoupling
- Routing and layout recommendations
- Compliance checklists

## **CONFIGURATION SPACE**

- Configuration space mappings
- Register description
- PCI MEM and PCI IO mappings building
- Expansion ROM
- Capability list
- Configuration transactions, IDSEL routing
- Local vs distant CFG transaction
- Generation of config transactions

## **PCI-TO-PCI TRANSPARENT BRIDGES**

- Bus numbering
- Address decode, transaction forwarding rules
- Distant configuration cycles
- Error management

## POWER MANAGEMENT

- Bus power state machine
- PCI function power state machine
- Programming interface

## PCI BASED INDUSTRIAL SPECIFICATIONS

- Passive bus PICMG PC
- CMC/PMC mezzanine boards, BUSMODE pins management
- CompactPCI introduction
- PC104+ introduction
- PC.MIP introduction

## Renseignements pratiques

**Durée : 3 jours**  
**Prix : 1650 € HT**



SARL au capital de 15400€ - SIRET 449 597 103 00026 - RCS Nanterre - NAF 722C - Centre de Formation : 19, rue Pierre Curie - 92400 Courbevoie  
Siège social et administration : 21, rue Pierre Curie - 92400 Courbevoie - Tél. 01 41 16 80 10 - Fax. 01 41 16 07 78

Dernière mise à jour du site: mar 22 mai 2012 10:50:29 CEST

<http://www.ac6-formation.com/>