



IC4 - PCI Express 3.0

This course covers PCI Express gen3 as well as gen1 and gen2

Objectives

- Packet switching benefits compared to shared busses are highlighted.
- The course explains the various traffic types that PCI Express supports.
- The use of virtual channels to match Quality of Service requirements is explained.
- The course describes the discovery sequence required to initialize the switches.
- The course details the various stages of the physical layer: 8b10b coding, scrambling, elastic buffer, clock recovery and link training sequence.
- The new features of the revision 2.0 and revision 3.0 are described, especially the sequence used to change either the speed or the link width.
- The course explains the new coding scheme used in PCIe 3.0.
- Event report to the host CPU through legacy interrupts, MSI or MSI-X is studied.
- Note that the course can be adapted to only cover PCIe 1.1 or PCIe 2.0.
- A lot of trainings have been developed on particular PCIe implementations, see our courses on FPGAs and SoCs.

A more detailed course description is available on request at guillaume.peron@ac6.fr

Prerequisites

- Knowledge of PCI / PCI-X is recommended.
- See our courses PCI, reference [IC1](#) and PCI-X, reference [IC3](#)

Plan

THE TRANSITION TO PACKET SWITCHING

- PCI bus limitations
- The hub link bus
- PCI-X
- Solutions to increase the performance : differential transmission, packet switching

INTRODUCTION TO PCI EXPRESS

- Topology
- Data Link Control and Management State Machine
- Transaction traffic types
- Quality of Service
- The physical layer

- Configuration space
- Switch logical view

THE PHYSICAL LAYER - LOGICAL SUB-BLOCK

- Overview of the Physical layer, highlighting the various units present in transmitter and receiver
 - Byte dispatching rules for multi-lane links
 - Purpose of scrambling
 - Elastic buffer operation
 - De-skew
- 8-bit / 10-bit coding (2.5 Gbps and 5.0 Gbps)
 - Data Byte encoding
 - Control symbol utilization
 - DC-balance through running disparity
- 128-bit / 130-bit coding (8.0 Gbps)
 - Block alignment, utilization of EIEOS
 - Clarifying how DC-balance is obtained
 - Framing tokens
 - Link equalization procedure
- Link Training and Status State Machine [LTSSM]
 - Reset signalling
 - Lane reversal, polarity inversion
 - Detect state
 - Polling state
 - Configuration state
 - Recovery state
 - L0, L0s, L1 and L2 states
 - Disabled, Loopback and Hot Reset states
 - Testing the transmitter
 - Compliance load board usage
 - Testing the receiver

THE PHYSICAL LAYER - ELECTRICAL SUB-BLOCK

- Interoperability criteria for 2.5, 5.0 and 8.0 Gbps
- Jitter budgeting and measurement
- Separate refclk architecture
- Transmitter specification, phase jitter filtering
 - 5.0 Gbps transmitter margining
 - Measurement setup for characterizing transmitters
 - De-emphasis
 - Rise and Fall times
 - PLL bandwidth and peaking
 - 8.0 Gbps transmitter equalization coefficient range and tolerance
- Receiver specification
 - Calibration channel characteristics
 - Return loss
 - Receiver compliance eye diagram
 - 8.0 Gbps post-processing procedure
 - Behavioural Rx equalization algorithms (CTLE, DFE)
- Skew
- Receiver detect
- Low power modes, Beacon signal

POWER MANAGEMENT

- Link state power management
- Native PCI Express power management mechanisms

- Relationship between function state and link state
- Power budgeting capability
- Slot power limit control
- Dynamic Power Allocation

PACKET ROUTING

- Operation of PCI-to-PCI transparent bridge
- Packet routing by the address
- Packet routing by the ID
- Packet routed implicitly
- Access Control Services
- Alternative Routing ID
- Multicast addressing

TLP ACKNOWLEDGEMENT

- Counters / timers present in the transmitter and the receiver
- Explaining the acknowledge protocol through sequences
- Sizing
- Cut-through switches

QUALITY OF SERVICE

- Introduction, traffic differentiation
- VC arbitration
- Port arbitration, switch model

FLOW CONTROL

- Overview, transmit credit principle
- Initialization, advertising infinite credits
- Credit update frequency
- Flow Control Packet
- Optimized Buffer Flush / Fill message
- Explaining the flow control protocol through sequences

TRANSACTION ORDERING

- PCI Producer / Consumer model
- Relaxed ordering permitted by PCI-X
- PCI Express transaction ordering rules
- Highlighting these rules through examples

PIPE INTERFACE

- Interface clocking and reset
- PHY-LINK interface signals
- Elasticity buffer mode
- Rx polarity
- Selecting transmitter voltage levels
- Rx status codes
- Low power states

PACKET FORMAT

- TLP format

- Poisoning a TLP, error forwarding
- Rules regarding read completions boundary
- TLP prefix usage
- TLP digest rules
- Processing hints

INTERRUPT MANAGEMENT

- PCI interrupt management
- Transporting legacy interrupts through PCIe messages
- Message Signaled Interrupts
- Benefits of MSI-X

ERROR MANAGEMENT

- PCI-like error management
- PCI Express basic error management
- PCI Express basic advanced error management
- Using completion status field to report an error

HOT PLUG

- Accessing a device through a slot
- Card attachment sequence
- Hot-plug events

THE CONFIGURATION SPACE

- Root Complex event collector
- PCI Express enumeration
- New features of PCIe 2.0 and PCIe 3.0:
 - PCI Express Enhanced Configuration Access Mechanism
 - Device serial number capability
 - Root Complex link declaration capability
 - Root Complex internal link control capability
 - ACS extended capability
 - Multicast extended capability

DEBUGGING A PCI EXPRESS SYSTEM

- Compliance lists
- The Serial Data Analyser from Lecroy, test of the physical layer
- Protocol analyser / exercicer from Lecroy
- Trace analysis

Renseignements pratiques

Duration : 4 days
Cost : 1950 € HT



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