



IP3 - USB 3.0

This course covers USB3.0 and related specifications: OTG 3.0, xHCI, UAS and AV classes

Objectives

- The course details the hardware implementation and clarifies the operation of 8b10b encoder/decoder.
- All tests required to qualify the physical layer are detailed.
- The course also covers the PIPE interface, which is used to interconnect the Link layer and the PHY.
- A lot of sequences are used to explain the flow control mechanism, the error recovery mechanism and packet acknowledgment.
- The dual operation of USB 2.0 and USB 3.0 is clarified, especially the initialization sequence used by the device to select the operation speed.
- The course explains all requirements regarding low power management, particularly the consequences on hub design.
- The enumeration is studied step by step.
- The one-day part on xHCI, UAS and AV classes are covered on request only.
- Note that this course is a mature course already delivered to main companies developing SoCs for wireless solutions.

A more detailed course description is available on request at info@ac6-training.com

Prerequisites

- Knowledge of USB 2.0 is required, see our course reference [IP2](#)
- For on-site courses, an additional day covering USB 2.0 fundamentals may be prepended to this USB 3.0 course.

Plan

SYSTEM ARCHITECTURE

- Dual-bus approach
- Dual simplex operation, concurrent IN and OUT transactions
- Explicitly routed packet traffic instead of USB 2.0 broadcast
- Multi-level link power management
- New features of data flow model
- Robustness

DATA FLOW MODEL

- USB 3.0 transaction model
- Low power link state transitions
- Latency tolerance messaging
- Bus interval adjustment

- Link-level power management
- Super-speed packet format
- Bulk transfers, stream ID

SOFTWARE ORGANIZATION

- Host Controller Driver, purpose of EHCI, xHCI
- USB driver
- Enumeration
- Client drivers
- Virtual communication between client drivers and endpoint through communication pipes
- Overview of UAS and Video Display new classes

USB OTG 3.0

- Objectives of OTG specification
- Session Request Protocol
- OTG 2.0 Host Negotiation Protocol
- Impact on PHY layer, voltage thresholds and timeouts
- Impact on Link and upper layers
- Differences between OTG 2 and OTG 3
- Embedded Host
- OTG 3 Role Swapping Protocol
- Symmetry, SSPC-OTG
- Defining who is the default Host through Port capabilities

PHYSICAL LAYER

- AC-coupled lines
- Receiver detection
- Low Frequency Periodic Signaling, utilization of LFPS
- Spread Spectrum Clocking
- 8b10b coding scheme
- Elasticity buffer
- Pre-emphasis, receiver equalization
- Lane polarity inversion detection
- Qualifying the physical layer, eye-diagrams
- Mathematical processing that must be performed in the oscilloscope
- Tests required by the USB Implementer Forum
- Loopback BERT

PIPE INTERFACE

- Interface clocking and reset
- 16- or 32-bit data bus width
- Rx polarity
- Selecting transmitter voltage levels
- Rx status codes
- Clock tolerance compensation
- Transmitting and detecting LFPS
- Low power states

LINK LAYER

- Flow control, header buffer credit
- Buffering for data and protocol layer informations
- Transmitter timers

- Packetization
- Specified encoded control sequences
- Packet replay in case of error detection
- Power-on reset, in-band reset
- Link training and status state machine, understanding the main important transitions
- Clarifying which transitions are required to enter test modes (loopback and compliance)

PROTOCOL LAYER

- End-to-end communication rules
- Burst of back-to-back data packets
- End-to-end flow control, NRDY / ERDY transaction packets
- Link management packet
- TP sequences, highlighting differences with USB 2.0
- Host flexibility in performing isochronous transactions

HUB

- Repeater / forwarder
- Routing outbound packets to explicit downstream ports
- Aggregating inbound packets to the upstream port
- Propagating time-stamp packet
- USB 3.0 new descriptors and requests

SUPER SPEED POWER MANAGEMENT

- Power states of links, devices and functions
- Driving the power management policy
- Related in-band protocol mechanisms
- Inactivity timers
- Enabling remote wake sources

ENUMERATION

- Device states
- Function suspend
- New commands: SetSel()
- Binary Device Object Store (BOS)
- SuperSpeed device capability
- Interface association
- SuperSpeed endpoint companion descriptor

EXTENSIBLE HOST CONTROLLER INTERFACE (xHCI)

- Host Controller hardware requirements
- Memory structures, buffer rings and TRBs
- Transfer ring, command ring, event ring
- Transaction scheduling
- Error detection and handling
- Device attachment / removal
- Utilization of doorbell
- Single Root I/O virtualization
- Debug capability

UAS CLASS

- Mass storage class specification

- SCSI architecture model
- Command queuing
- SAM-4 command identifier
- Transport protocol, command Information Unit
- Utilization of USB 3 streams
- Task management
- Transport protocol services
- Pipe usage class descriptor

AUDIO / VIDEO CLASS

- AV profile definition, Basic Device Profile
- AVCore, AVCluster, Hierarchy
- AVFunction, AVData
- Multi-channel audio
- Track selector
- Channel configuration
- TV set example
- Feature unit VideoControls
- Video Processing Unit
- AVControl interface
- AV synchronization types, asynchronous, synchronous, adaptive
- AV description document
- Request and control sequences, HDMI controls
- Support of HDCP 2

Renseignements pratiques

Duration : 4 days
Cost : 1950 € HT



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