



R0 - ARM fundamentals

This course covers ARM architecture V4T and V5TE fundamentals

Objectives

- ARM modes state machine is detailed, clarifying the register banking mechanism.
- Subtleties of ARM instruction set are covered, such as conditional execution, addressing modes, operand shifting.
- Interworking between ARM and Thumb instruction sets is explained.
- The exception mechanism is studied, particularly interrupt nesting.
- The course also covers ARM926EJ-S cache and MMU operation.

Labs are run under RVDS

A more detailed course description is available on request at info@ac6-training.com

Prerequisites

- Basic knowledge of CPU or DSP.
- This one-day course has been designed to meet the pre-requisites of ARM11 and Cortex-A/R courses. This is a summary of ARM7/9 course.

Plan

THE ARM V4T / V5TE ARCHITECTURE

- ARM operation modes
- The ARM registers set, register organization summary according to the current mode
- Program Status Registers
- Exception handling, vector table, automatic switch into ARM mode

ARM AND THUMB INSTRUCTION SETS

- Conditional execution and flags
- Branch instructions
- The barrel shifter
- Immediate constants
- Single register data transfer
- Stack management
- Register access in Thumb
- ARM architecture V5TE new instructions

ARM / THUMB INTERWORKING

- Switching between states
- Mixing ARM and Thumb subroutines
- ARM to thumb veneer
- Thumb-to-ARM veneer
- Interworking calls

EXCEPTION HANDLING

- Exception priority
- Vector table instructions
- Chaining exception handlers
- FIQ vs IRQ
- Example C interrupt handler
- Issues when reenabling interrupts
- C nested interrupt example
- Data abort with memory management
- Adjusting the return address

MEMORY MANAGEMENT & PROTECTION

- Introduction to page management
- Translation Lookaside Buffer
- Benefits of Fast Context Switch Extension
- ARM926 MMU
- Organization of page descriptor tables
- Configuration & control through CP15

MEMORY SUBSYSTEMS

- Cache basics
- Hit under miss and its consequence: out of order abort
- Highlighting data flows between main memory and caches
- Write buffer
- Tightly coupled memories

Renseignements pratiques

Duration : 1 days

Cost : 700 € HT



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