



HX3 - Xilinx - Designing with Ethernet MAC logicores

This course covers the implementation of the Ethernet MAC Xilinx logicores.

Objectives

- Utilize various Ethernet cores, used either in standalone mode or as a peripheral in a processor-based design.
- Determine the appropriate core to use.
- Develop software to drive the core and achieve desired functionality.
- Integrate hard and soft IP into the EDK.

- This course is delivered by Mr Guillaume Péron, a worldwide expert of Gigabit Ethernet, who has also developed trainings on 802.3 / 802.1 specification and Gigabit Ethernet implementation in AMCC, Intel, Freescale processors and Marvell switches.

Xilinx software (ISE) is used to synthesize and implement practical examples, Mentor Graphics ModelSim is used for simulation.

A more detailed course description is available on request at info@ac6-training.com

Prerequisites

- Knowledge of Ethernet is recommended, see our course reference N1.
- Experience with Xilinx ISE and EDK software tools is recommended.

Plan

DAY 1

- Ethernet basics
- Network protocols
 - Lab1 : Analyzing Ethernet frames
- Physical layer
- Local Link interface
 - Lab2 : VLAN and Jumbo frames
- Xilinx EMAC solutions

DAY 2

- Lab3 : Implementation
- EMAC and EMAC lite
 - Lab4 : EMAC peripheral in loopback mode
- GEMAC
- TEMAC

- Lab5 : TEMAC in loopback mode
- 10GE MAC
- Lab6 : Analyzing 10GE MAC frames

Renseignements pratiques

Duration : 2 days
Cost : 1250 € HT



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