



## **This course covers the implementation of the Xilinx PCIe block.**

### **Objectives**

- An introduction to PCI Express protocol is done at the beginning to be able later to understand the operation of the back-end bus.
- The course details the parameterizing of the PCI Express core.
- User interfaces are deeply detailed.
- Management of errors and interrupts is studied through examples.
- Guidelines to design the user logic are provided.
- The course targets hard PCI Express cores in the Virtex-6 and Spartan-6 FPGAs.

*Xilinx software (ISE) is used to synthesize and implement practical examples, Mentor Graphics ModelSim is used for simulation.*

*A more detailed course description is available on request at [info@ac6-training.com](mailto:info@ac6-training.com)*

### **Prerequisites**

- Good knowledge of PCIe gen2 protocol, see our course reference [IC4](#)
- Good knowledge of VHDL.
- Experience with simulation tools such as Mentor Graphics ModelSim.
- Basic knowledge of Xilinx ISE software.

### **Plan**

#### **1st DAY**

##### **PCI EXPRESS PROTOCOL OVERVIEW**

- Introduction to PCI Express
- Transactions types and categories
- Address Space Map and Configuration Space
- PCI type0 basics, PCI express capability structure

##### **PCI EXPRESS AND XILINX CORE GENERATOR**

- Selecting link speed and width
- Address decoding logic, BAR registers setting
- TLP buffer sizing

- Power management configuration
- Optional capability structures

### **SIMULATING A PCIE DESIGN**

- Identifying simulation points
- Simulation Methods
- Building TestBench

### **CONNECTING LOGIC TO THE CORE &#8211; LOCAL LINK OR AXI INTERFACE**

- Clocking and reset
- Common Transaction Interface Signals
- Cut-through vs Store & Forward operation
- Migrating to the integrated block for PCI Express v2.x from v1.x
- AXI interface signals description
- Managing control flow information to optimize the user logic

### **2nd DAY**

### **DESIGNING A SIMPLE ENDPOINT APPLICATION**

- PIO example description
- Endpoint application and PCI Express core connection
- Local Link or AXI interface
- Accessing configuration space from user logic

### **COMPLIANCE AND DEBUGGING**

- Chipscope Pro Description
- Compliance Testing
- Tracking the transitions in the LTSSM (Virtex-6)
- Dynamic reconfiguration (Virtex-6)

### **ERRORS AND INTERRUPTS**

- PCIe Error management, related registers
- Introduction to legacy interrupts, MSI and MSI-X
- Collaborating with PCIe block to generate error messages
- Triggering interrupts, MSI or MSI-X from user logic
- Explaining the benefits of MSI / MSI-X with respect to legacy interrupts

## **Renseignements pratiques**

**Duration : 2 days**  
**Cost : 1250 € HT**



SARL au capital de 15400€ - SIRET 449 597 103 00026 - RCS Nanterre - NAF 722C - Centre de Formation : 19, rue Pierre Curie - 92400 Courbevoie  
Siège social et administration : 21, rue Pierre Curie - 92400 Courbevoie - Tél. 01 41 16 80 10 - Fax. 01 41 16 07 78

Last site update: Tue 22 May 2012 10:50:29 AM CEST

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