



HX1 - Xilinx - Virtex-5 FXT Embedded Processor Block

This course covers the parameterizing of the Embedded Processor Block present in Virtex-5 FXT Xilinx FPGAs.

Objectives

- This course describes in depth the PPC440 core, including the optional FPU.
- Differences between PPC440 and PPC405 are highlighted.
- Practical labs provide CPU performance estimations through fixed-point and floating-point FFTs.
- The course also details the operation of the internal crossbar connecting the PPC440, external PLB masters, LocalLink DMA channels to PLB slaves and memory.
- The address decoding logic and arbitration mechanisms are explained through the EDK embedded processor block parameterizing wizard.
- The LocalLink protocol is studied in order to clarify how data are transferred between hard LocalLink DMA channels and external soft IPs.
- The course focuses on error recovery mechanisms that can be used during debug time to understand and fix bus errors.
- This course has been designed by Mr Guillaume PERON, processor expert, developing courses for IBM Microelectronics and AMCC for more than 10 years.

A more detailed course description is available on request at info@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Plan

PPC440x5 CORE, HIGHLIGHTING DIFFERENCES WITH PPC405

- 7-stage pipeline operation, dual issue superscalar pipeline
- Speculative execution, guarded memory
- Serialization
- Caches, 64-way associativity, cache line locking
- Using a part of the cache to store transient information
- Clarifying the instruction and data path
- Cache programming interface
- Memory Management Unit
- Translation Lookaside Buffer initialisation
- Load / store buffer, speculative loads, msync and mbar instructions
- Floating Point Unit (external soft IP), compliance with IEEE754
- Float MAC instructions

- Interrupt management
- Reset clock and power management interfaces
- Debug interfaces : JTAG and trace

CORE BUS INTERFACES

- Architecture of a SOC designed with Virtex-5 FXT, hard IPs vs soft IPs
- DCR controller, direct addressing vs indirect addressing
- Dual DCR master arbitration
- Detailing the difference between PLB4 and PLB3
- Transaction types : single data, line, burst
- Connecting a coprocessor to the APU 128-bit load/store interface
- Concurrent operation with the core pipeline
- Detail of the interface between APU controller and Fabric Coprocessor Module
- FCM user-defined instructions
- Exception management

INTERNAL CROSSBAR

- Block diagram (Muxes and demuxes)
- 5 PLB slave interfaces, 3 for the core + 2 for soft PLB masters
- 4 full-duplex LocalLink channels with built-in DMA control
- 1 high-speed memory controller interface
- 1 master interface to connect an external slave soft IP
- Issues with transaction ordering, sync attribute, specification configuration to support PCI/PCIe
- Describing the various arbitration algorithms
- Error management, error syndrome registers, related interrupts

DMA CONTROLLER

- Scatter / gather operation, direct mode vs chained mode
- Setting the channel priority
- Asynchronous interface to LocalLink soft IP
- Interrupt mechanism, coalescing
- Dynamic descriptor appending
- Software / device driver considerations

MEMORY CONTROLLER

- Generation of intermediate addresses during bursts
- Constant burst length set by the user through a control register
- Row and bank detect logic
- ECC management
- Implementing the Xilinx DDR2 memory controller

PARAMETERIZING THE EMBEDDED PROCESSOR BLOCK

- Static configuration through attributes
- Dynamic reconfiguration through DCRs
- Crossbar configuration
- DMA channel configuration
- Generating the platform by using PlatGen

Renseignements pratiques

Duration : 3 days

Cost : 1650 € HT



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