



## IC5 - RapidIO 2.1

**This course covers the RapidIO interconnect version 2.1**

### Objectives

- Packet switching benefits compared to shared busses are highlighted.
- The course explains the various traffic types that RapidIO supports: Input / output, Message and GSM.
- Mechanisms like error recovery and flow control are explained through various sequences.
- The course covers all features present in the RapidIO 2.1 specification, such as end-to-end flow control, multicast programming, data streaming and virtual output queuing extensions.
- CC-NUMA cache coherency mechanism is studied.
- The course describes the discovery sequence required to initialize the switches.
- Details of RapidIO interfaces present in Freescale and IDT devices are provided to explain how theoretical statements are actually implemented .

*A more detailed course description is available on request at [info@ac6-training.com](mailto:info@ac6-training.com)*

### Prerequisites

- Experience of a digital bus such as PCI or VME.

### Plan

#### **THE TRANSITION TO PACKET SWITCHING**

- PCI bus limitations
- PCI-X bus
- Solutions to increase the performance : differential transmission, packet switching, gigabit serdes

#### **INTRODUCTION TO RapidIO**

- System view
- Layer model, features of logical, transport and physical layers
- Purpose of control symbols
- Request / response sequence

#### **THE INPUT / OUTPUT LOGICAL TRAFFIC**

- Accessing memory mapped address ranges
- Accessing the configuration space
- Atomic transactions
- Maintenance transaction

- Transaction ordering
- Transfer efficiency calculation

## **THE MESSAGE PASSING LOGICAL TRAFFIC**

- Interconnection of host domains
- Message vs doorbell
- Transfer efficiency calculation
- Detail of message passing implementation in Freescale netcomm devices

## **CACHE COHERENCE**

- Cache basics
- Snooping basics
- Data shared by DMA and CPU through a RapidIO fabric
- Data shared by CPUs connected to a RapidIO fabric
- GSM transactions, coherence domains
- The CC-NUMA approach
- Analysis of various cache coherency sequences

## **DATA STREAMING LOGICAL SPECIFICATION**

- Data path vs control path requirements
- Mechanism of transporting an arbitrary protocol over a standard RapidIO interface
- Traffic streams
- Support for PDU of 64 kB through segmentation and reassembly
- Class of services and virtual queues
- IP over RapidIO

## **LOGICAL LAYER FLOW CONTROL**

- Types of congestion
- Controlled flow list
- XON-XOFF controls on transaction request flows
- XON-XOFF counters
- Ordering rules

## **THE TRANSPORT LAYER**

- Common transport layer
- Packet routing through the network based on destination ID
- Programming interface to read / write the routing tables
- Multicast extensions (RapidIO 1.3)
- Hardware support for the duplication of posted write packets
- Setting a list of egress ports in a multicast mask list
- Associating a destination ID with the multicast mask

## **SYSTEM BRINGUP**

- System exploration and initialization
- Winning host
- System enumeration API
- Enumeration time-out
- Hardware abstraction layer

## **OVERVIEW OF THE PHYSICAL LAYER**

- Alignment rules
- Packet acknowledgement
- Control symbols vs packet
- Multicast event

## **ERROR MANAGEMENT**

- Packet protection through CRC
- Early processing of packets
- Study of various sequences explaining the ability of RapidIO to recover from errors automatically by hardware
- Software aspects, link maintenance request and response
- RapidIO 1.3 added requirements in physical and logical layers
- Error reporting thresholds
- Port behaviour when error rate failed threshold is reached
- Drop packet enable
- System software notification of errors

## **PACKET PRIORITY AND FLOW CONTROL**

- Transaction ordering rules
- Mapping flowID into 2-bit priority
- Receiver based flow control, retry mechanism
- Transmitter based flow control, management of transmit credits
- Deadlock prevention

## **THE LP-LVDS 8/16 INTERFACE**

- Transfer protocol, packet and control symbol delineation
- Insertion of symbols within packets
- Use of eye diagram to specify the electrical interface
- Training pattern

## **THE LP-S 1x/4x INTERFACE**

- Features or sublayers PCS and PMA
- Single VC mode vs multiple VC mode, purpose of VC status control symbol
- Bandwidth allocation
- The 8b/10b encoder / decoder
- Special characters, comma detection
- Symbol and packet delimitation
- Idle sequence, scrambling, descrambler synchronization
- Lane synchronization
- 1.25Gbaud, 2.5Gbaud, and 3.125Gbaud LP-Serial Links
- 5Gbaud and 6.25Gbaud LP-Serial Links
- Pulse response channel modelling
- High frequency jitter vs wander
- Transmit emphasis tuning
- Use of eye diagram to specify the electrical interface
- Port initialization

## **VIRTUAL OUTPUT QUEING EXTENSIONS**

- Head Of Line blocking
- Congestion message
- Traffic staging
- Relationship with VC
- VOQ backpressure extended features register block

## Renseignements pratiques

**Durée : 3 jours**

**Prix : 1650 € HT**



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