

## This course PowerQUICC II devices, MPC825X, MPC826X, MPC827X, MPC828X families

### Objectives

- This course describes the various data paths existing in the PowerQUICC II.
- Cache coherency protocol is introduced in increasing depth.
- The 32-bit G2 core is viewed in detail, especially the MMU and the cache.
- The boot sequence and the clocking are explained.
- A long introduction to SDRAM operation is done before studying the SDRAM controller.
- An in-depth description of the PCI controller is performed.
- The course highlights both hardware and software implementation of fast Ethernet controllers.
- The USB interface is also detailed.
- The course describes the Time Slot Assigner initialization in order to process E1 frames.
- The ATM VCI/VPI address lookup mechanism through CAM memory is studied.
- The ATM traffic shaper is explained through examples.

*A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of complex peripherals, such as FCC and SDRAM controller.*

*• They have been developed with Diab Data compiler and are executed under Lauterbach debugger.*

*A more detailed course description is available on request at [formation@ac6-formation.com](mailto:formation@ac6-formation.com)*

### Prerequisites and related courses

- Experience of a 32-bit processor or DSP is mandatory.
- The following courses could be of interest:
  - Ethernet and switching, reference cours [N1 - Ethernet and switching](#)
  - PCI, reference cours [IC1 - PCI 3.0](#)
  - USB Full Speed High Speed and USB On-The-Go, reference cours [IP2 - USB 2.0](#)

### Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

### Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

### Modalités d'évaluation

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.

- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés
- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.
  - En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

## Plan

### INTRODUCTION TO PowerQUICC II

#### OVERVIEW

- Enhancements compared to PowerQUICC I
- Pinout, pin groups
- Block diagram : characteristics of each of the 3 internal modules G2 core, SIU and CPM
- Application examples

### THE G2 CORE

#### THE INSTRUCTION PIPELINE

- G2 implementation
- Branch processing unit
- Branch instructions
- Coding guidelines

#### DATA PATHS

- Load / store architecture
- Load / store buffers
- Sync and eieio instructions

#### CACHES

- Cache basics
- Cache locking
- L1 caches
- Cache coherency mechanism
- Basic snoop requests
- Management of cache enabled pages shared with DMAs
- Cache related instructions
- Cache flush routine

#### SOFTWARE IMPLEMENTATION

- PowerPC architecture specification, the 3 books UISA, VEA and OEA
- Addressing modes, load / store instructions
- Integer instructions
- Rotate instructions
- IEEE754 basics
- Floating point arithmetical instructions
- The PowerPC EABI
- Linking an application with Diab Data

## **THE MMU**

- Thread vs process
- Introduction to real, block and segmentation / pagination translations
- Memory attributes and access rights definition
- Virtual space benefit
- TLB organization
- Segmentation
- Pagination
- MMU implementation in real-time sensitive applications

## **THE EXCEPTION MECHANISM**

- Save / restore registers SRR0/SRR1, rfi instruction
- Exception management mechanism
- Registers updating according to the exception cause
- Requirements to allow exception nesting

## **THE DEBUG PORT**

- JTAG emulation
- Real time trace requirements
- Code instrumentation
- Hardware breakpoints

## **THE PLATFORM CONFIGURATION**

## **POWER, RESET AND CLOCKING**

- Power on /down sequence
- Power management control
- Reset causes
- Reset configuration word
- Booting a multi-PQII system
- Clocking

## **THE 60X BUS**

- 60X bus operation
- 60X bus cycles overview
- Dynamic bus sizing
- Configuration registers

## **THE MEMORY CONTROLLER**

- Arbitration between internal and external masters
- The 60X to Local bus bridge
- Introduction to DRAM / SDRAM
- UPM implementation
- GPCM implementation,
- SDRAMs machine description
- Bank vs page interleaving

## **THE PCI BRIDGE**

- Arbitration, bus parking, arbitration algorithm
- Supported bus commands
- Definition of inbound and outbound address ranges

- Bus errors processing
- Messaging

## **THE SIU MODULE**

- System protection and configuration
- PIT and SWT system timers
- Interrupt controller
- Sequence required to find the interrupt cause

## **GENERAL PURPOSE PERIPHERALS**

- Programming GPIOs
- General purpose timers

## **THE COMMUNICATION PROCESSOR MODULE**

### **INTRODUCTION TO CPM**

- Synchronization between G2 core and CP, command register
- DPRAM organization
- Introduction to buffer descriptors and buffer management
- Chaining descriptors
- IDMA and SDMA channels

### **THE SERIAL INTERFACE**

- NMSI versus TDM
- Supported protocols and max data rate
- Transmit and receive clock selection
- Baud rate generators
- Interrupt management

### **THE MULTI CHANNEL CONTROLLERS**

- Focus on the difference between Time Slot and Channel
- Programming Super channels
- HDLC channel parameters
- Interrupt queues

### **THE SERIAL COMMUNICATION CONTROLLERS**

- Data encoding /decoding selection
- Hardware flow management
- UART on SCC
- HDLC on SCC
- 10 Mbps Ethernet on SCC

### **THE I2C CONTROLLER**

- I2C protocol explanation
- Clock stretching
- Description of the I2C controller implemented in the PowerQUICC II

### **THE SPI CONTROLLER**

- SPI protocol
- Transmit and receive sequence

## **FAST ETHERNET CONTROLLER**

- - MAC operation
- 802.3u basics
- MII vs RII interface
- Hash tables utility
- CSMA/CD vs full duplex Ethernet, pause packet
- Remote monitoring

## **THE USB 1.1 CONTROLLER**

- USB integration in the MPC827X/8X
- Host controller limitation
- Hardware implementation
- Host vs Device operation

## **THE ATM CONTROLLER [On request]**

## **ATM BASICS**

- Main features
- ATM benefit compared to X.25 or ISDN
- UNI and NNI network interfaces
- Cell format
- Virtual connection
- Layer model
- AAL1 layer: circuit emulation
- AAL3/4: used by the service providers
- AAL5: packet transfer
- Connection establishment

## **ATM TRAFFIC MANAGEMENT**

- The 5 service classes defined by the ATM forum : CBR, VBRrt, VBRnrt, UBR, ABR
- The QoS ATM attributes
- Traffic shaping

## **MPC826X ATM CONTROLLER**

- Utopia 2 hardware interface : multi-PHY control
- APC unit
- VCI/VPI of incoming cells lookup
- Performance monitoring
- ATM/TDM interworking
- Interrupts queue
- Enhanced features of the MPC828X

## **Renseignements pratiques**

**Renseignements : 5 jours**