[redacted]

This course covers all NXP MCUs belonging to the Kinetis families K10, K20, K30, K40 and K60

Objectives

- This course has 5 main objectives:
  - Describing the hardware implementation and highlighting the pitfalls
  - Describing the ARM Cortex-M4 core architecture
  - Becoming familiar with the IDE and low level programming
  - Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units
  - Describing independent I/O modules and their drivers.
- Note that this course has been designed from the architecture of the most complex Kinetis device, the K60.
  - Consequently, a chapter has been designed by Acsys for each possible integrated IP.
  - So the customer can build its own course outlines from the topics described hereafter.

- Products and services offered by ACSYS:
  - ACSYS has developed FFTs (floating-point and fixed-point) optimized for ARM cores, based on SIMD instructions supported by the Cortex-M4.
  - Contact formation@ac6-formation.comto obtain informations about the performance of these FFTs.
  - ACSYS is able to assist the customer by providing consultancies. Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.
  - ACSYS has also an expertise in FreeRTOS or MQX porting and uIP /LWIP stack or Interniche stack integration.

This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Prerequisites and related courses

- This course provides an overview of the Cortex-M4 core. Our course reference cours RM3 - Cortex-M4 / Cortex-M4F implementation details the operation of this core.
- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference cours IP2 - USB 2.0
  - Ethernet and switching, reference cours N1 - Ethernet and switching
  - IEEE1588, reference cours N2 - IEEE1588 - Precise Time Protocol
  - CAN bus, reference cours IA1 - CAN bus

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Modalités d'évaluation

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.
- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés
- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.
  - En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

Plan

ARCHITECTURE OF KINETIS MCUs

- ARM core based architecture
- Description of K10, K20, K30, K40 and K60 SoC architecture
- Clarifying the internal data and instruction paths: AHB-lite interconnect, peripheral buses, AIPD bridges
- AMBA-to-IPS Re-use IP: ColdFire (AIPS) Controller
- Integrated memories
- SoC mapping

THE ARM CORTEX-M4 CORE

- V7-M core family
- Core architecture
- Freescale on-chip instruction and data cache
- Thumb-2 instruction set
- Exception behavior
- Basic interrupt operation, micro-coded interrupt mechanism
- Memory Protection Unit

V7-M DATA SIGNAL PROCESSING INSTRUCTIONS

- Multiply instructions
- Packing / unpacking instructions
- SIMD packed add/sub instructions
- SIMD combined add/sub instructions
- SIMD multiply and multiply accumulate instructions
- SIMD sum absolute difference instructions
- SIMD select instruction
- Saturation instructions
- Floating point unit
- Cortex Microcontroller Software Interface Standard (CMIS)

BECOMING FAMILIAR WITH THE IDE

- Acsys covers 3 iDEs: CodeWarrior, IAR and GCC / Lauterbach
- Thus the customer has just to indicate which one he has chosen
  - Getting started with the IDE
  - Parameterizing the compiler / linker
  - Creating a project from scratch
  - C start program

PROGRAMMING AND DEBUGGING

- Debug interface
- Programming

RESET, POWER AND CLOCKING

- Reset
- Clocking
- Operation modes

INTERNAL INTERCONNECT

- Crossbar switch
- Hardware Memory Protection Unit
- eDMA

HARDWARE IMPLEMENTATION

- Power pins
- Pinout
- GPIO module

INTEGRATED MEMORIES

- Flex memory, this module is not implemented in all Kinetis devices
- Internal SRAM

MEMORY INTERFACE

- Each Kinetis family supports either a subset or all the following controllers
- FlexBus
- eSDHC
- NAND flash controller
- DRAM controller

TIMERS

- Low Power Oscillator
- COP
- External Watchdog Monitor
- Periodic Interrupt Timer
- Low Power Timer
- Flex Timer
- Carrier Modulator Transmitter

ANALOG MODULES

- 16-bit Analog-to-Digital Converter and Programmable Gain Amplifier
- 12-bit Digital-to-Analog Converter
- Voltage Reference VREF
- High-Speed Comparator HSCMP
- Programmable Delay Block PDB

SECURITY AND INTEGRITY

- Hardware Cyclic Redundancy Check
- Memory-Mapped Cryptographic Acceleration Unit (MMCAU)
- Pseudo Random Number Generator
- Secure Real Time Clock

- DryIce and Tamper Detect
- Cryptographic Acceleration Unit

CONNECTIVITY AND COMMUNICATION

- DSPI
- UART
- I2C
- CAN modules
- USB
- Fast ethernet with IEEE1588
- ISO7816 smartcard interface
- I2S audio interface

USER INTERFACES

- Segment LCD controller
- Graphics LCD controller
- Capacitive touch sensing

Renseignements pratiques

Renseignements : 5 jours